IN THE CLAIMS:

The current claims follow. For claims not marked as amended in this response, any difference in the claims below and the previous state of the claims is unintentional and in the nature of a typographical error.

1. (Currently Amended) A method of testing a circuit under design having a plurality of functional elements and having a plurality of clock environments, at least one signal passing from one clock environment to another clock environment in said circuit, said method comprising steps of:

modelling at least one of the plurality of functional elements to have an unknown state as an output for a predetermined time after a timing event of a clock signal;

simulating said circuit to identify one or more of said functional elements that is a source of propagation of said unknown state; and

determining which of said plurality of functional elements is a synchroniser to thereby identify if there is a synchronisation problem for said at least one signal passing from said one clock environment to said another clock environment so as to identify if a functional element which is a source of propagation of said unknown state is a hazard or a synchroniser.

2. (Previously Presented) The method as claimed in claim 1, wherein in the simulating step, a plurality of simulations are carried out with one or more of the following clock signals in said one clock environment and said another clock environment:

a) the same clock frequency and phase;

b) the same clock frequency and different phase; and

c) different clock frequencies.

3. (Currently Amended) ~~A method as claimed in claim 1,~~ A method of testing a circuit under design having a plurality of functional elements and having a plurality of clock environments, at least one signal passing from one clock environment to another clock environment in said circuit, said method comprising steps of:

modelling at least one of the plurality of functional elements to have an unknown state as an output for a predetermined time after a timing event of a clock signal;

simulating said circuit; and

determining which of said plurality of functional elements is a synchroniser to thereby identify if there is a synchronization problem for said at least one signal passing from said one clock environment to said another clock environment, wherein in said simulating step, said one clock environment and said another clock environment have the same clock frequency and phase.

4. (Previously Presented) The method as claimed in claim 1, wherein in said simulating step, said one clock environment and said another clock environment have the same clock frequency and a first phase difference.

5. (Previously Presented) The method as claimed in claim 4, wherein said simulating step is repeated with said one clock environment and said other clock environment having the same clock frequency and a second phase difference.

6. (Previously Presented) The method as claimed in claim 5, wherein said second phase difference is of opposite polarity to said first phase difference.

7. (Previously Presented) The method as claimed in claim 1, wherein in said simulating step, said one clock environment and said another clock environment have a different clock frequency.

8. (Currently Amended) The method as claimed in claim 1, wherein said determining step comprises a step of tuning the predetermined time such that ~~an~~ the unknown state propagates through only a part of said circuit.

9. (Previously Presented) The method as claimed in claim 1, wherein said determining step comprises using warnings to identify a functional element which is a source of the unknown state and determining if said source has a synchronising function in said circuit.

10. (Previously Presented) The method as claimed in claim 1, wherein the simulating and determining steps are repeated a plurality of times.

11. (Previously Presented) The method of claim 1, wherein said determining step is arranged to identify if a functional element which is a source of propagation of said unknown state is a hazard or a synchroniser.

12. (Previously Presented) The method as claimed in claim 1, wherein in said determining step, wherein if a functional element is determined to be a synchroniser, said functional element is arranged such that the unknown state is not propagated.

13. (Previously Presented) The method as claimed in claim 1, wherein if a first functional element and a second functional element are identified as a first synchroniser and a second synchroniser, said second synchroniser is arranged such that the unknown state is not propagated.

14. (Currently Amended) ~~The method as claimed in claim 1,~~ A method of testing a circuit under design having a plurality of functional elements and having a plurality of clock environments, at least one signal passing from one clock environment to another clock environment in said circuit, said method comprising steps of:

modelling at least one of the plurality of functional elements to have an unknown state as an output for a predetermined time after a timing event of a clock signal;

simulating said circuit; and

determining which of said plurality of functional elements is a synchroniser to thereby identify if there is a synchronization problem for said at least one signal passing from said one clock environment to said another clock environment, wherein a first element is identified as a synchroniser, comprising a step of determining propagation of an unknown state for the remainder of ~~the~~ a clock cycle by presence of different values before and after the unknown state presented at an input of the synchroniser.

15. (Previously Presented) The method as claimed in claim 1, wherein said circuit is represented at gate level.

16. (Previously Presented) The method as claimed in claim 1, wherein said circuit is designed in HDL.

17. (Previously Presented) The method as claimed in claim 1, wherein said method is carried out on a simulation tool.

18. (Previously Presented) The method as claimed in claim 1, wherein said timing event comprises a clock edge.

19. (Previously Presented) The method as claimed in claim 1, wherein said plurality of functional elements comprise logic gates.

20. (Previously Presented) The method as claimed in claim 19, wherein said logic gates comprise flip-flops.

21. (New) A computer-readable medium having computer-executable components for a method of testing a circuit under design having a plurality of functional elements and having a plurality of clock environments, at least one signal passing from one clock environment to another clock environment in said circuit, wherein, when run on a computer, said program is configured to perform the following steps:

modelling at least one of the plurality of functional elements to have an unknown state as an output for a predetermined time after a timing event of a clock signal;

simulating said circuit to identify one or more of said 15 functional elements that is a source of propagation of said unknown state; and

determining which of said plurality of functional elements is a synchroniser to thereby identify if there is a synchronisation problem for said at least one signal passing from said one clock environment to said another clock environment so as to identify if a functional element which is a source of propagation of said unknown state is a hazard or a synchroniser.